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Design and Implementation of Embedded Logic Flip-Flop for Low Power Applications

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Abstract

This paper introduces a high performance hybrid flip-flop which can merge logic functions with normal flip-flop operation. The proposed Embedded Logic Flip-flop (ELFF) will reduce the implementation area, power dissipation and delay. The ELFF has 20% better performance in terms of power dissipation and delay compared to the existing Dual Dynamic Node Flip-flop-Embedded Logic Module (DDFF-ELM). It will be a good component for including in VLSI standard cell library for designing high performance chips for low power applications. The performance comparisons and analysis were done with Mentor EDA tool in Taiwan Semiconductor Manufacturing Company (TSMC) 180nm process.

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Keywords: Flip-flop; Embedded logic; Area; Speed; Delay; Power dissipation; ELFF; DDFF; ELM

1. Introduction

Sequential logic circuits are the building blocks of Finite State Machines (FSM). Nearly all sequential logic circuits using today are of two types; clocked logic or synchronous logic. Sequential logic circuits (Fig. 1) consist of combinational logic circuits and memory elements. Combinational logic circuits have no capacity to store information. Memory element is a device which can remember the value indefinitely, or change value on command

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from its inputs. Flip-flop is the basic memory element in sequential logic, which changes its state on clock signals. Latch circuits are not suitable in synchronous logic circuits.

In synchronous systems, high speed processing is achieved through deep pipelining. Flip-flops are an important component for achieving this. The latency associated with the pipelining is based on the Data to Output (D to Q) delay in flip-flops. Complementary Metal Oxide Semiconductor (CMOS) flip-flop can be of static or dynamic design styles, depending upon how it retains its stored values against charge leakage. Several researches are going on for the improvement in the speed of operation of flip-flops. According to the requirement of the system, the designer has to consider all the parameters such as speed, power consumption, area and noise stability, while choosing a flip-flop structure. For sequential logic circuits, D flip-flops are used to store the output of logic blocks. This discrete combination can be converted into a merged logic, within the flip-flop. Advantage of using logic flip-flop shows a reduction in delay, power dissipation and implementation area.

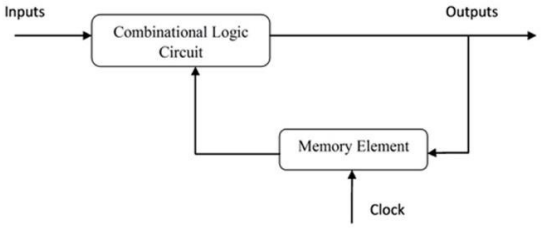

Fig. 1. Sequential logic circuit.

In the design of sequential circuit, a major challenge is to design a D flip-flop. A large number of various hybrid flip-flop architectures were published in recent years. The flip-flops considered for analysis are Hybrid-Latch Flip-flop (HLFF) [1], Semi Dynamic Flip-flop (SDFF) [2], Conditional Data Mapping Flip-flop (CDMFF) [3, 4, 5], Cross Charge Control Flip-flop (XCFF) [6] and Dual Dynamic node Flip-flop (DDFF) [7]. The DDFF is a good component for the designing a flip-flop featuring embedded logic functions. The DDFF has better Power Delay Area Product (PDAP) [8] compared to other hybrid flip-flop architectures. The details of the existing logic flip-flop architectures are given in the section 2, details of proposed Embedded Logic Flip-Flop are given in section 3. Results and discussions on simulation and implementation are given in section 4.

2. Existing Logic Flip-Flop Architectures

Not too many attempts have been made to design a flip-flop with logic capability. The concept of logic flip-flop is shown in Fig. 2. ELFF is a fast and small implementation compared to discrete combinations of static logic and a flip-flop. For an N-input logic function, transistors are needed. The merging allows the elimination of one or more levels of logic from the path leading to the flip-flop. The result is a reduction in the total latency of the designed circuit.

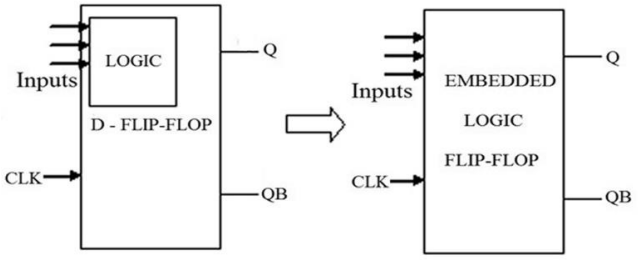

Fig. 2. Concept of logic flip-flop.

SDFF is the classical hybrid flip-flop which can capable of incorporating logic functions within the flip-flop. The logic functions are incorporated in the dynamic front-end. Merging of logic functions allows the elimination of one gate delay from the critical path. Thereby the entire delay will be reduced. Also the transistor count gets reduced.

The structure of DDFF-ELM is shown in Fig. 3. Compared to DDFF, the transistor driven by the data input is replaced by the nMOS logic. Also the CLKB signal is fed to NM2. DDFF-ELM has two dynamic internal nodes. These nodes drive the output pull-up and pull-down nodes separately. Since one of the dynamic nodes is switched on during one clock cycle. An unconditional shut-off mechanism is provided at the dynamic front-end.

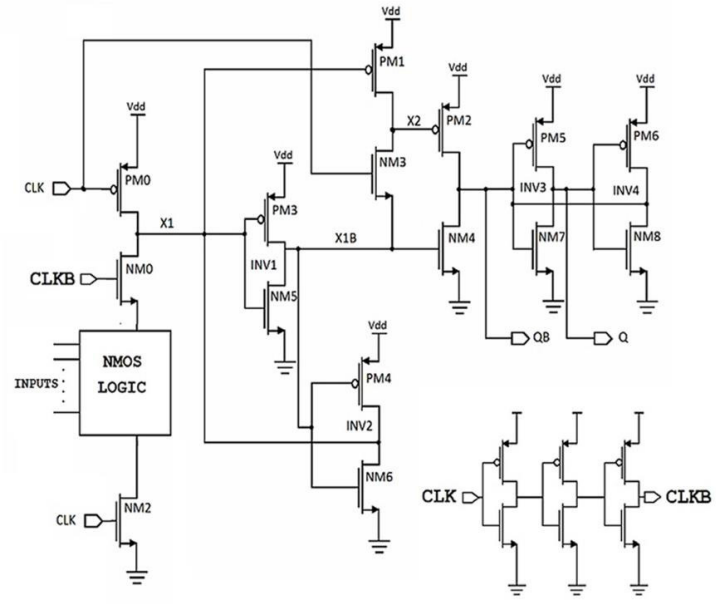

Fig. 3. DDFF – ELM.

3. Proposed Embedded Logic Flip-flop

The structure of the proposed Embedded Logic Flip-flop is shown in Fig. 4. It is a revised structure of DDFF-ELM. The inverter pairs of DDFF-ELM are replaced with a NAND based reset-circuit. As far as synchronous designs are concerned, reset functionality is inevitable. Here, an area and power efficient method to incorporate asynchronous reset functionality was implemented to the proposed ELFF. The asynchronous reset functionality is achieved through active-low asynchronous-reset (rst) function[9] with a NAND based cross-coupled inverter reset-circuit. When rst signal is held low for a particular period of time, the node X1 is pulled high and the output Q is pulled low by the respective reset circuits. The proposed ELFF design has the ability to incorporate logic functions within the flip-flop.

The operation of the ELFF can be divided into two phases: evaluation phase and pre-charge phase. The CLK is high at evaluation phase and low at the pre-charge phase. The actual latching occurs during the CLK and CLKB is at 1–1 overlap condition, during the evaluation phase (Fig. 5). If nMOS logic provides a discharge path for node X1 to ground through NM2 prior to this overlap period, this changes the state of the first cross-coupled inverter. This causes node X1B to go high. Then the output QB is discharged through NM4. The first cross-coupled inverter keeps the node X1 at low level for the rest of the evaluation phase. Thus the node X2 is held high during the entire evaluation period by the pMOS transistor PM1. When the CLK becomes low, the circuit enters to pre-charge phase (Fig. 6). Then the node X1 is pulled high through PM0, switching the state of first cross-coupled inverter. During this time, node X2 is not driven by any transistor, and then it holds the charge dynamically. The outputs at node QB maintain their voltage level through the second cross-coupled inverter[9]. If nMOS logic will not give a discharge path

to ground, node X1 remains high and node X2 is pulled low through NM3 as the CLK goes high. Thus, node QB is charged high through PM2 and NM4 is held off. At the end of the evaluation phase, as the CLK signal falls low, node X1 remains high and node X2 holds the charge dynamically.

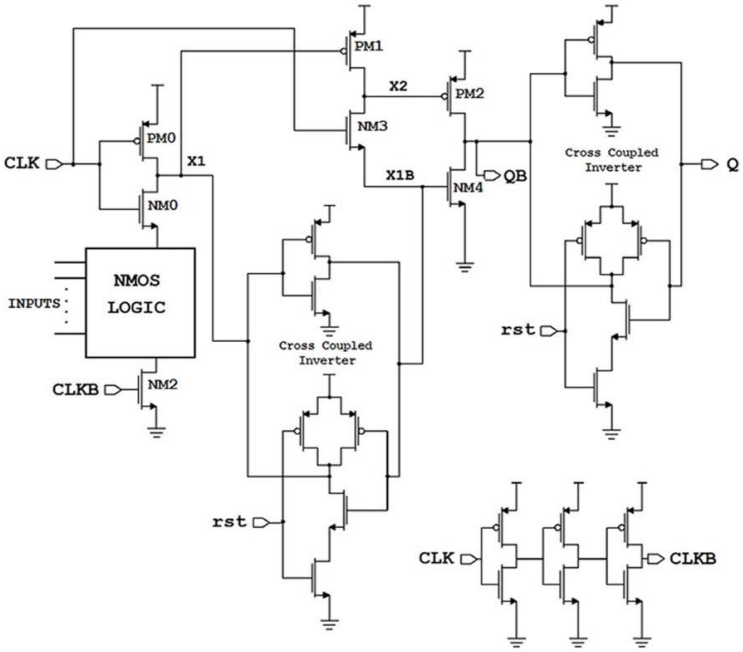

Fig. 4. Proposed ELFF.

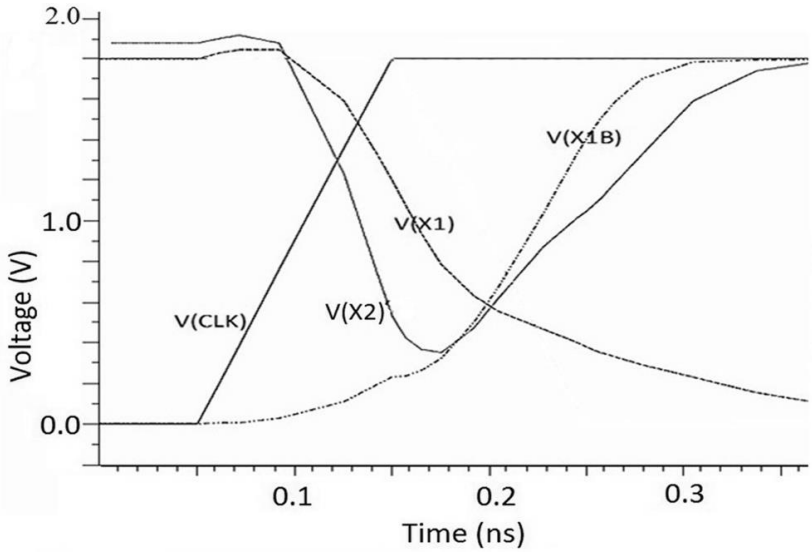

Fig. 5. ELFF evaluation phase.

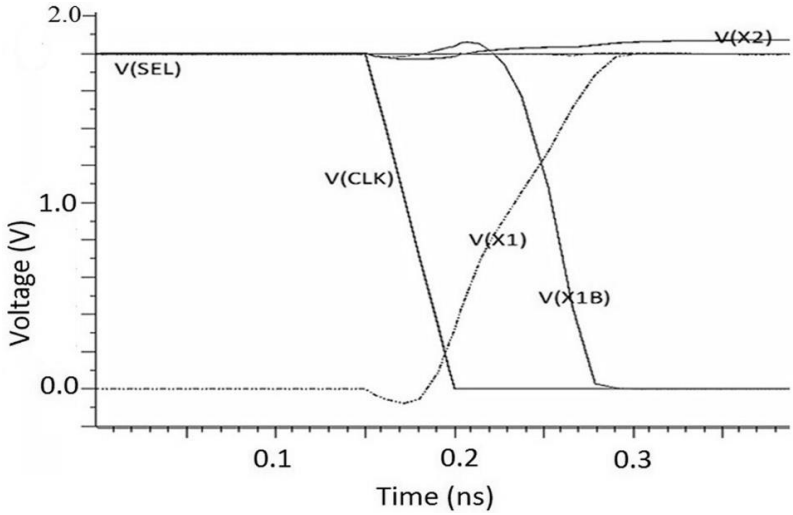

Fig. 6. ELFF pre-charge phase.

Shift registers are a type of sequential logic circuit, mainly for storage of digital data. Each stage (flip-flop) in a shift register represents one bit of storage capacity. Therefore the number of stages in a register determines its storage capacity. Each stage has one multiplexer connected to a D flip flop. Each multiplexer has the same control inputs (S1S0) so that, multiplexers select the same input. Similarly all the D flip flops have the same clock, and data change synchronously[10]. 4-bit universal shift register has all the capabilities listed above. The four multiplexers have two common select inputs S1 and S0 and they select the appropriate inputs for the D flip-flop. Table 1 shows the register operation depending on the select inputs of multiplexers.

When S1S0 = 00, input 0 is selected and the present value of the register is applied to the D inputs of the flip-flops. As a result, here will not be any change in the register value. When S1S0 = 01, input 1 is selected and circuit connections are such that it operates as a right shift register. When S1S0 = 10, input 2 is selected and circuit connections are such that it operates as a left-shift register. When S1S0 = 11, the data on the parallel input lines are transferred to the register simultaneously and it is a parallel load data transfer operation.

Table 1. Mode Control and Register Operation.

Mode Control (S1S0)	Register Operation
00	No Change
01	Right Shift
10	Left Shift
11	Parallel Load

4. Results and Discussions

The circuit schematics were drawn in the Mentor Graphics Design Architect tool. Mentor Graphics ELDO simulator is used for both pre-layout and post- layout simulation. The flip-flops were simulated in 180 nm/1.8V CMOS process at 20 MHz clock frequency. Input signals are provided with a rise-time and fall-time of 100ps using ELDO simulator. The D to Q delay is measured from EZ wave viewer of ELDO simulator.

4.1 Pre- Layout Simulation Results of DDFF-ELM and ELFF

DDFF-ELM with different logic functionalities are compared with proposed ELFF at 1.8V VDD. The obtained results were tabulated in Table 2. The performance of embedding various logics such as NAND, NOR, 2×1 multiplexer Logic etc. are compared. All the circuits were designed and analyzed its operational speed and power consumption in TSMC EDA process using Mentor Graphics EDA tools. The proposed ELFF uses same reset logic in both cross-coupled inverters, compared to existing DDFF-ELM. It shows ELFF has better performance compared to DDFF-ELM. It is found the proposed ELFF have almost 20% better performance compared to DDFF-ELM.

Table 2. Performance Comparison of DDFF-ELM and ELFF.

Logic Function	DDFF – ELM Power Dissipation (pW)	DDFF – ELM D to Q delay (ns)	ELFF Power Dissipation (pW)	ELFF D to Q delay (ns)	ΔPDP
NAND Logic	424.2	0.182	411.1	0.156	16.9%
NOR Logic	471.9	0.167	426.0	0.145	22.5%
2×1 multiplexer Logic	511.2	0.244	472.8	0.212	19.7%

4.2 Pre- Layout Simulation Results of Universal Shift Register

The performance comparison of discrete circuit and ELFF based 4-bit universal shift register are shown in Table 3. Discrete circuit uses master slave flip-flops and multiplexers. In ELFF based 4-bit universal shift register, each individual block is an ELFF multiplexer. Only 164 transistors are required for the ELFF implementation of same circuit. Due to this reduction in transistor count, the total power dissipation gets reduced. The performance is compared on the change in Power Delay Product (ΔPDP). Because of the reduction in gate delays, total D to Q delay gets reduced. Simulation waveform of 4-bit Universal Shift Register using ELFF is given in Fig. 7.

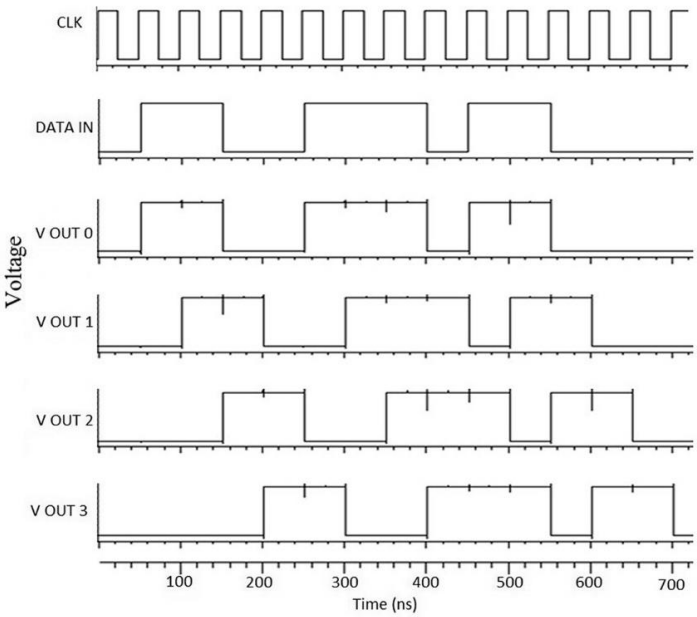

Fig. 7. Simulation waveforms of universal shift register using ELFF in right shift mode.

Table 3. Performance Comparison of Discrete Circuit and ELFF.

Circuit	No. of transistors	Power dissipation (pW)	D to Q delay (ps)	ΔPDP
Discrete 4-bit Universal Shift Register	328	2870.1	200	80.2%
4-bit Universal Shift Register using ELFF	164	691.0	164	

4.3. Layout

After the schematic entry and design verification, Mentor Graphics Pyxis Layout Editor (IC station) is used for Schematic Driven Layout (SDL) of ELFF. As the name suggests, the layout is drawn with the help of schematic entry. IC Station is a software package from Mentor Graphics for the IC design, physical verification and layout. Various masks are created using IC Station, to produce fully customized digital IC. It perform some behavioral testing and extract physical parameters from the design. After Layout, the physical verification steps which includes Design Rule Check (DRC) and Layout Versus Schematic Check (LVS) are done. The DRC tool of Mentor Graphics IC station checks whether the layout conforms to the design rules. For this, TSMC 180nm rule is selected. The LVS tool of Mentor Graphics IC station checks, whether the layout matches to the circuit schematic.

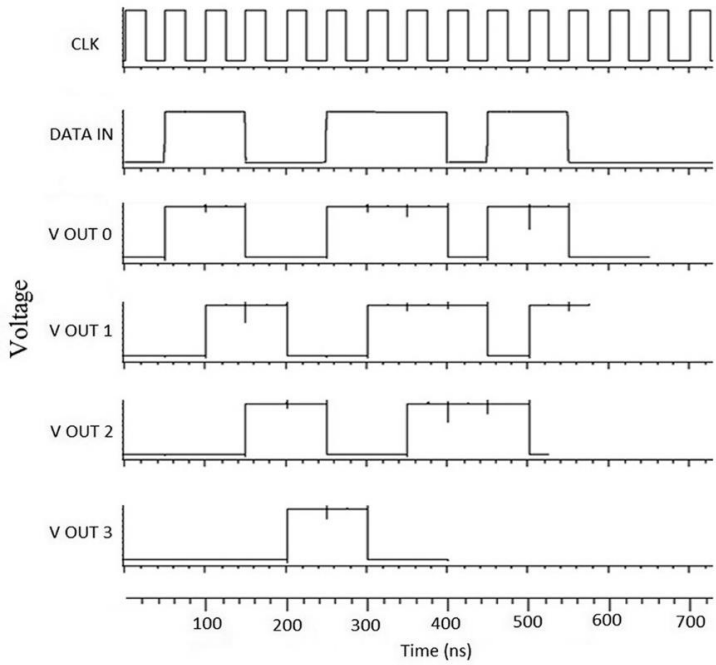

Fig. 8. Post layout simulation waveforms of universal shift register using ELFF.

4.4. Parasitics extraction and Post Layout Simulation

The (parasitic Extraction) PEX results are obtained as Detailed Standard Parasitic Format (DSPF) format. In EDA process, PEX is the calculation of the parasitic effects in both the designed circuits and the required wiring interconnects of a circuit. The procedure for post layout simulation is identical to that for simulating from the schematic view. Moreover, both types of simulations have the same simulation results. Post layout simulation

waveforms of universal shift register using ELFF are given in Fig.8. The difference in delay obtained after post layout simulation of ELFF is negligible.

5. Conclusions

The proposed Embedded Logic Flip-flop has a hybrid flip-flop architecture that combines the merits of dynamic and static structures. ELFF is provided with an asynchronous output reset, which is capable of easy implementation of counters and registers. ELFF has better performance in terms of power dissipation and delay compared to the existing DDFF-ELM structure. ELFF exhibits better performance of 20% compared to the existing logic flip-flop architectures. It has been shown that the usage of ELFF in sequential circuits is beneficial in low power and high speed applications. This flip-flop will be a good component to include in a standard cell library for designing high performance sequential circuits.

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